REMARKS

Reconsideration is respectfully requested.

In this response, new claims 85-92 have been added. Accordingly, Claims 78-92 are pending in the application for consideration. Support for the newly added claims may be found at least on page 6, lines 17-19, page 11, lines 13-15, page 12, lines 1-5 of the present specification.

In the instant Office Action, Claims 80-84 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of U.S. Patent No. 6,140,200; and Claims 78-79 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,753,548 (hereinafter '548 patent).

In response to the obviousness-type double patenting rejection of claims 80-84, a Terminal Disclaimer is submitted herewith to overcome the rejection. Withdrawal of rejection of claims 80-84 is requested. Claims 80-84 are now in condition for allowance.

Applicant respectfully traverses the rejection of claims 78-79 under 35 U.S.C. §102(b) as being anticipated by the '548 patent.

Claim 78 recites, in part, a method of forming a void region associated with a substrate, comprising forming a sacrificial mass over the substrate, forming a layer over the mass, and subjecting the mass to conditions wherein a ***component of the mass*** *transports from the mass into the layer* to form *a mixture of the layer and the component*, and wherein the transporting the

component *leaves an enclosed void region between the substrate and the mixture of the layer and the component.*

As discussed at Figure 2 and page 9, lines 1-6 of the present specification, a component from mass 18 interacts with layer 20 to form a region 22 comprising a mixture of the component and the material of the layer 20. Thus, as recited in claim 78 and shown in Figure 2, a component of the sacrificial mass transports from the sacrificial mass into the layer that is formed over the sacrificial mass layer to form a mixture of the layer and the component. Claim 78 further recites that transporting the component from the sacrificial mass leaves an enclosed void region between the substrate, the mixture of the layer and the component. Void region 24 is formed between the substrate 12 and region 22.

The '548 patent discloses a method for making shallow source/drain junctions for P-channel field effect transistors using boron difluoride ion implantation while masking the boron difluoride ions over the P-channel gate electrodes. This is done in order to eliminate fluorine outgassing. See Col. 1, lines 15-23.

More particularly, Figure 1 of the '548 patent shows a cross-sectional view of P-channel FET depicting the problem of void formation between a P-doped polysilicon gate and the overlying interlevel dielectric (ILD) layer. As disclosed in Col. 2, lines 15-35, a gate oxide 18 is formed on a substrate 10 and a P^+ doped polysilicon layer 20 is patterned on the gate oxide layer 18. When ILD layer composed of the silicon nitride layer 34 and the BPSG layer 36 are

deposited and high temperature processing is carried out, the fluorine atoms 5 outgas from the surface of the gate electrode 20 resulting in void formation at the P^+ doped polysilicon/ILD interface.

However, the Office Action refers to Figure 1 and Col. 2, lines 25-35 of the '548 patent and alleges that a component of the sacrificial mass transports from the mass into the layer that is formed over the sacrificial mass to form a mixture of the layer and the component. The Office Action further alleges that transporting the component of the sacrificial mass leaves an enclosed void region between the substrate and the mixture of the layer and the component of the sacrificial mass. Applicant respectfully disagrees in view of the following:

As noted above, in the '548 patent, fluorine atoms 5 outgas from the surface of the gate electrode 20 resulting in void formation at the interface of the P^+ doped polysilicon 20 and the ILD layer 34. Accordingly, a component of the gate oxide 18 (which the Office Action asserted as the sacrificial layer of claim 78) is neither transported nor used to form a mixture as recited in claim 78. Since no component is transported from the gate oxide 18, other issues of using the transported component to form a mixture, forming a void region do not even arise.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference, based on the foregoing, it is clear that the '548 patent does not anticipate claim 78.

Furthermore, claim 78 recites "...wherein transporting the component leaves an enclosed void region between the substrate and the mixture of the layer and

the component." See Figure 2 of the present specification wherein the void region 24 is formed between the substrate 12 and the region 22.

In contrast to claim 78, since no mixture of layer 34 and a component of gate oxide 18 is formed, subsequently forming a void region between the substrate and the mixture of the layer 34 and a component of gate oxide 18 does not even arise. As such, in the '548 patent, a void region 5 is shown as formed between polysilicon gate electrode 20 and ILD layer 34.

In view of the above, Applicant respectfully submits that claim 78 is not anticipated by the '548 patent. Claims 79 and 85-90 depend from Claim 78 and further limit the scope of claim 78 in a patentable sense. Claims 79 and 85-90 are therefore allowable. New independent claim 91 is patentably distinct over the '548 patent at least for reasons set forth above with regard to claim 78. Claim 91 is also patentable as, in addition to the above-noted deficiencies, the '548 patent fails to teach or suggest that the rate of transport of the sacrificial material into the layer is a function of rate of diffusion of the component from the sacrificial material into the layer. Claim 92 depends from claim 91 and is therefore allowable. New claims 85-92 are therefore in condition for allowance. A notice to that effect is respectfully requested.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested. While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is requested that the Examiner contact the undersigned.

Respectfully submitted,

Dated: July 30, 2003

By: K. Satheesh

Satheesh K. Karra
Reg. No. 40,246